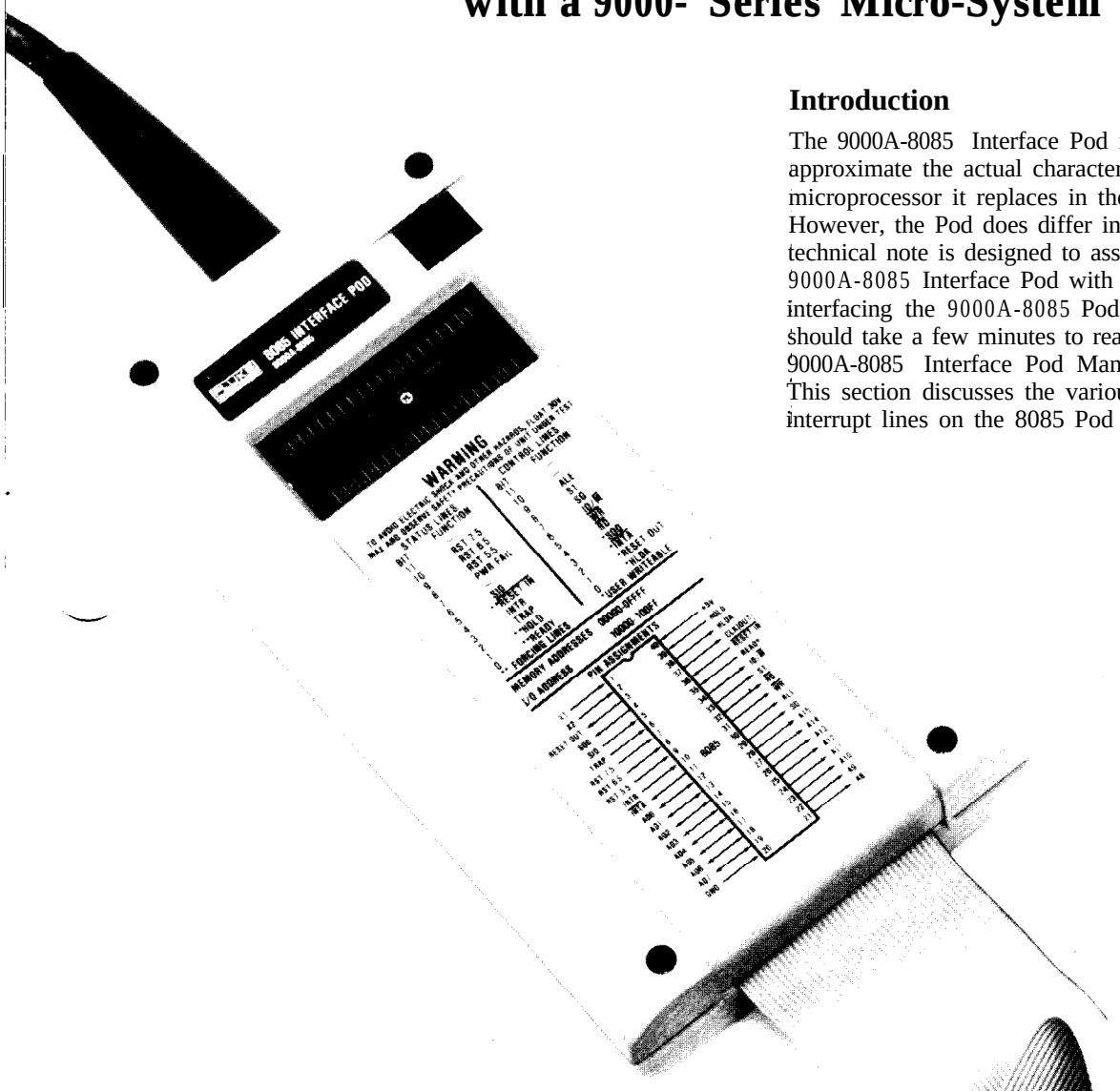
FLUKE

Technical Data

Application Information B0151

Guide to 8085 Microprocessor-Based System Testing with a 9000- Series Micro-System Troubleshooter



Introduction

The 9000A-8085 Interface Pod is designed to approximate the actual characteristics of the 8085 microprocessor it replaces in the UUT (Unit Under Test). However, the Pod does differ in some respects. This technical note is designed to assist in using the 9000A-8085 Interface Pod with a UUT. Prior to interfacing the 9000A-8085 Pod to a UUT, the user should take a few minutes to read Section 3 of the 9000A-8085 Interface Pod Manual (pages 3-l thru 3-8). This section discusses the various enable, forcing and interrupt lines on the 8085 Pod and their operation.

The 8085 Clock Circuitry

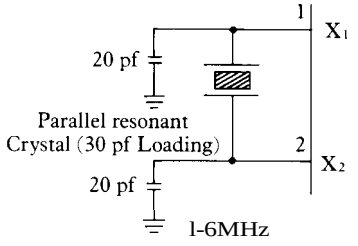
The 8085 internal clock circuit is designed to accommodate four different types of clock sources (see Figure 1). In many applications. an external clock source is desired and can be used for the microprocessor timing. Two different clock circuits are used in this mode depending on the clock duty cycle and the clock frequency (Figure lc and 1d). When operating with the circuit in Figure lc at close to 6 MHz, it is very critical that nothing be connected to the **X2** input of the 8085 microprocessor. This input is very sensitive to shunt capacitance from the X_I input and any additional capacitance between the **X2** input and the X_I input or any other 8085 pin can reduce the maximum frequency of operation for this mode.

The Model 9000A-8085 Interface Pod incorporates an 8085-2 (10 MHz) microprocessor, so it can simulate the UUT's microprocessor as closely as possible. In order to implement all clock modes, both X_I and **X2** inputs are provided in the flat cable to the UUT microprocessor socket and this introduces additional capacitive coupling (or load) to the **X2** input. When attempting to use the Pod in the clock mode shown in Figure lc in the 4-6 MHz range, the 8085 clock may not function properly due to this added capacitive load. This effect is displayed on the 9000-Series Troubleshooter display as an intermittent or continuous "POD TIMEOUT" message indicating that the 8085 microprocessor within the Pod is not functioning properly. To verify that this is the cause, connect an oscilloscope to the CLOCK OUT signal at the 8085 UUT socket (pin #37) and check the frequency, period, and shape of the clock signal. If the clock signal appears normal, the system contains some other problem. If the clock signal is absent, intermittent, or at the wrong frequency, this may be the cause. This is easily corrected for testing purposes by converting the clock mode from that shown in Figure lc to that shown in Figure Id. If the inverted polarity of the signal at the X_I input is available, this is easily accomplished by jumping this inverted signal to the **X2** input. If this signal is not available, a simple adaptor may be constructed from a 40 pin DIP socket or 40 pin "wire-wrap" socket and a 74LSO4 Hex Inverter IC (or equivalent) as shown in Figure 2.

This adaptor is then inserted between the UUT's microprocessor socket and the 40 pin plug on the Pod's cable. It provides the **X2** input as the complement of the signal at the X_I pin and will work for l-10 MHz clocks on 8085-based systems. Whenever other 8085-based systems with one of the other clock modes are

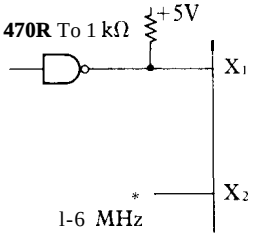
DRIVING THE X_I and X_2 INPUTS

A.



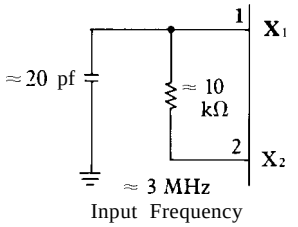
The user may drive the X_I and X_2 inputs of the 8085 with a crystal, an external clock source or an RC network as shown.

C.



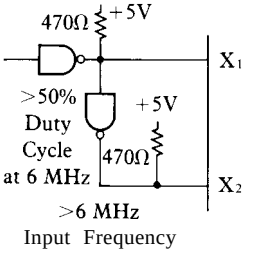
(Duty Cycle at 6 MHz: 25-SO%)
*With an external clock source, X_2 should be left floating.

B.



RC Mode causes a large drift in clock frequency because of the variation in on-chip timing generation parameters. Use of RC Mode should be limited to an application which can tolerate a wide frequency variation.

D.



This circuit may be used when the clock input has >50% duty cycle at 6 MHz.

Figure I

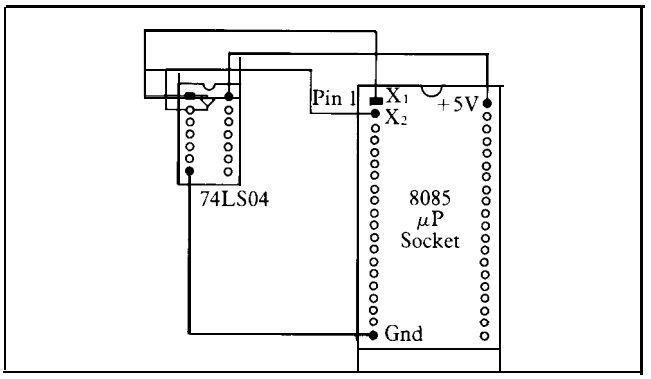


Figure 2

encountered, simply unplug the adaptor and use the standard 9000A-8085 Interface Pod.

"LEARN" and the Multiplexed Bus of the 8085

The LEARN algorithm of the Micro-System Troubleshooter automatically determines the locations of ROM, RAM and I/O by performing write and read operations to all possible memory addresses.

Addresses are tested in 64 byte blocks and those that are identifiable are classified as RAM, ROM or I/O using the following rules:

RAM Blocks of memory that are at least 64 continuous bytes long, in which all bits are read-writeable and all locations are distinct (i.e., writing to any location will not affect the content of any other location of the 64).

ROM No bits are read-writeable, and at least one byte appears to be "fully-decoded," (i.e., each location is distinct from every other location).

I/O One or more bits are unconditionally read-writeable, but one or more of the conditions for RAM are not met. The bits that are read-writeable are the reported I/O bits.

The LEARN algorithm analyzes the data read and eliminates certain types of data that fail the above three tests. Addresses containing only the following types of data are therefore not reported.

a. All bits of each address are logic zero, e.g., LEARN reads data from unused addresses when "pull-down" devices are connected to the data bus.
b. All bits of each address are logic one, e.g., LEARN reads data from unused addresses when "pull-up" devices are connected to the data bus or that found in unused ROM space.
c. The data byte at each address matches exactly the low order byte of the address word.
d. Certain other strictly repetitive patterns that occasionally occur.

The 8085 differs from many microprocessors in that it incorporates a multiplexed data/address bus. The data byte is multiplexed with the low order eight bits of the address word on a shared eight line bus. In a typical READ operation, the 8085 first places the low order eight bits of the address word on the bus for external circuitry to latch, then enables the external circuitry to drive the bus with the data to be read.

For those address locations that are not used in a particular UUT, the data bus appears as shown in Figure 3.

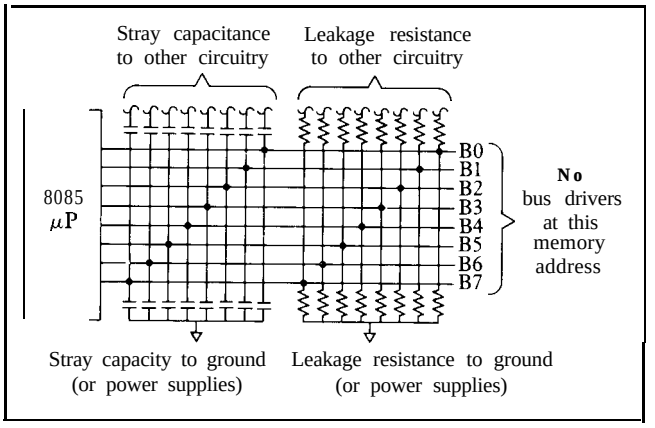


Figure 3

During a read operation to one of these unused addresses, the 8085 first places the low order eight bits of the address word on this bus, then attempts to read an eight bit data byte from this bus. Under most circumstances the data read from this "floating" bus will be one of the easily eliminated types discussed above; however, it is difficult to control the stray capacitance and leakage resistance of the bus. Depending on these parasitic values, the data can appear as something other than the 'trivial' data. Bus lines with low value pull-up or pull-down devices quickly change to the pulled level before the 8085 performs the remainder of the READ operation. Bus lines with high impedance pull-up or pull-down devices (or none at all) change state slowly, and may still retain the low byte of the address at the instant the 8085 is completing the READ operation. In either of these cases, the LEARN algorithm will recognize this condition and eliminate these addresses from the reported memory map.

However, because these parasitic parameters are difficult to control (dust accumulation or a wet fingerprint can represent a significant amount of leakage resistance), it is possible for one or more of the data lines to "float" in a logic direction different than the others. This causes the

READ operation to obtain data that appears as acceptable data and the LEARN algorithm to report a block of ROM data (since the data "appears" as ROM data would). The data read is very dependent on the sequence and timing of the READ operations. The sequence of operations in ROM test is different than in LEARN and thus the non-existent ROM addresses will usually fail the ROM test, even when done on a known good UUT. This ROM data is usually reported as many small 64 byte or 128 byte blocks and thus is easily recognizable and eliminated by using the VIEW ROM and DELETE keys on the Micro-System Troubleshooter. This characteristic only appears in the LEARN algorithm because LEARN by its very nature must access all possible microprocessor address space, while the UUT or the Troubleshooter under normal operation never accesses the unused address space.

A method of eliminating these many small blocks of "false" ROM from being reported by LEARN is to provide low value pull-up or pull-down devices on the data bus with an adapter similar to that shown in Figure 4. (Resistors with a value between 1 kΩ and 20 kΩ are usually adequate for this purpose.) This can easily be implemented with a 40 pin socket adapter that plugs into the 8085 socket (similar to the socket adapter previously mentioned) or can be a clip-on device that attaches to another device on the microprocessor data bus (all eight data lines and either + 5 volts or ground must be available). If the system design includes bus-buffers, the pull-up or pull-down devices are attached to the same side of the buffers that other bus drivers are, i.e., the same side as the RAM and ROM components.

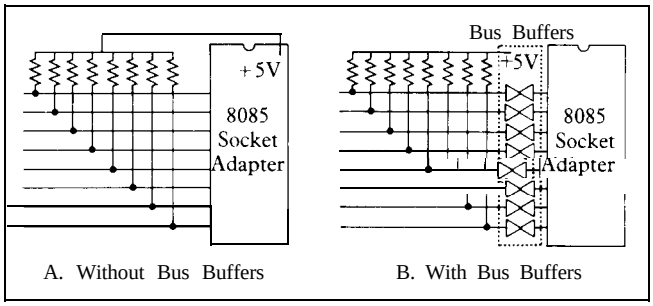


Figure 4

Input Loading Differences

The 8085 microprocessor has three input pins that interrupt processor operation (READY, HOLD and TRAP) and a fault on any of these three lines can halt processor operation and thus stop, Pod operation. For this reason the Pods have been designed with a high-speed logic gate on each of these inputs to allow the user to disable these inputs for testing. This low power Schotky input has a higher input current requirement than the MOS input of the 8085. The microprocessor has a 10 μA input current requirement on these inputs, while the Pod has a standard 400 μA low power Schotky TTL requirement for a low input. When not using these inputs, some UUT's may use 10 kΩ or even 100 kΩ pull-down resistors which work with the microprocessor but supply insufficient logic low current for the 8085 Pod. This causes the Troubleshooter to display one of two messages, "Active Force Line" or "Active Interrupt". These inputs can easily be disabled using the 9000-Series Troubleshooter SET-UP mode or by clipping a low-value resistor (approximately 1 kΩ) in parallel with the existing pull-down resistor.

Marginal UUT Considerations

The 8085 Pod is designed to approximate, as closely as possible, the actual characteristics of the 8085 microprocessor it replaces in the UUT. However, the Pod does differ in some respects. In general these have to do with noise, propagation delay and slight loading differences, and usually tend to make marginal UUT problems more visible. A UUT may operate marginally with the actual microprocessor installed, but tend to exhibit errors with the Pod plugged in. The Pod differences tend to make marginal UUT problems more obvious and easier to troubleshoot. Different UUT and Pod operating conditions that may reveal marginal problems are described in Section 3-12 of the 8085 Pod manual.

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Printed in U.S.A. BOlSlA-OlU82076E EN